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FAIRCHILD SEMICONDUCTOR™

October 1987
Revised April 2001

# MM74C922 • MM74C923
# 16-Key Encoder • 20-Key Encoder

## General Description

The MM74C922 and MM74C923 CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The 3-STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

## Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- 3-STATE output LPTTL compatible
- Wide supply range: 3V to 15V
- Low power consumption

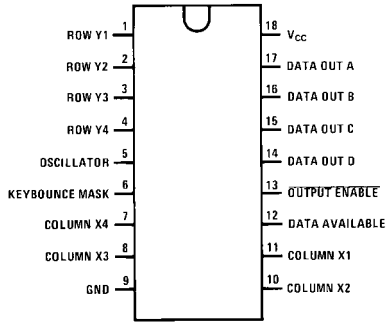
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| MM74C922WM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| MM74C922N | N18B | 18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| MM74C923WM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| MM74C923N | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

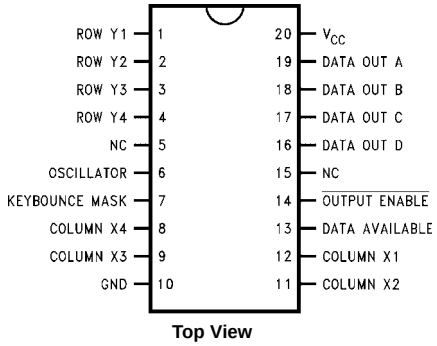
## Connection Diagrams

**Pin Assignment for DIP**




**Top View**
**MM74C922**

**Pin Assignment for SOIC**




**Top View**
**MM74C922**

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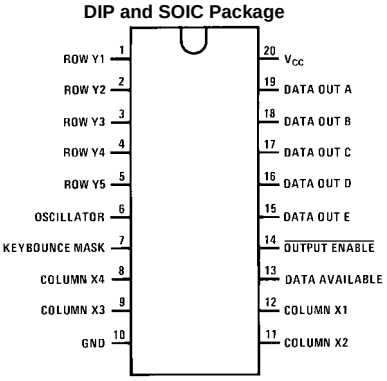
## Connection Diagrams (Continued)

**Pin Assignment for DIP and SOIC Package**




**Top View**
**MM74C923**

## Truth Tables

(Pins 0 through 11)

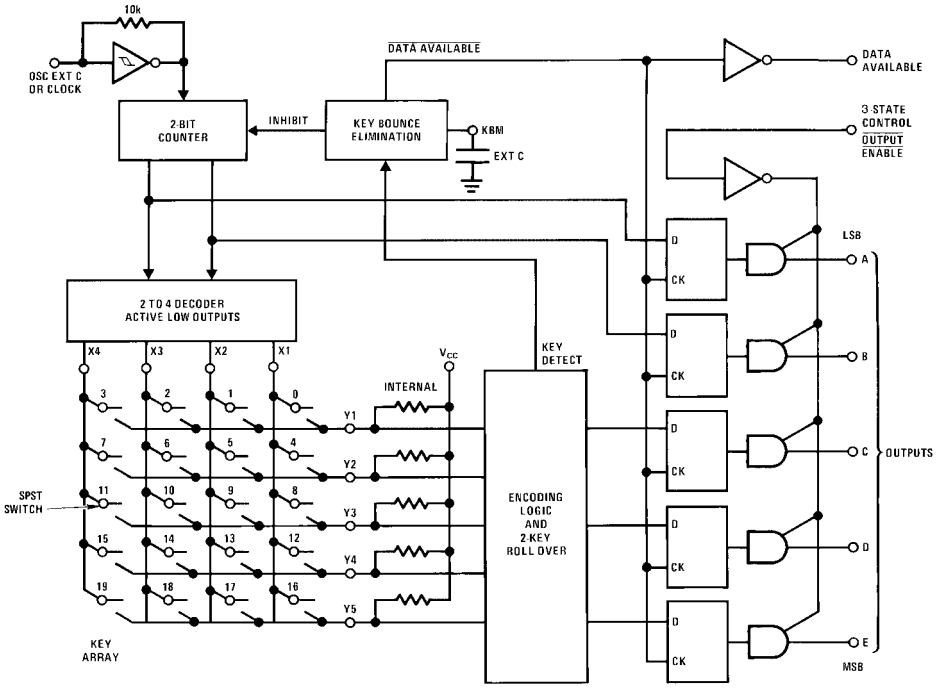
| Switch Position | | 0 Y1, X1 | 1 Y1, X2 | 2 Y1, X3 | 3 Y1, X4 | 4 Y2, X1 | 5 Y2, X2 | 6 Y2, X3 | 7 Y2, X4 | 8 Y3, X1 | 9 Y3, X2 | 10 Y3, X3 | 11 Y3, X4 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | | | | | | | | | | | | | |
| A | A | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| T | B | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| A | C | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| O | D | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| U | E (Note 1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| T | | | | | | | | | | | | | |

(Pins 12 through 19)

| Switch Position | | 12 Y4, X1 | 13 Y4, X2 | 14 Y4, X3 | 15 Y4, X4 | 16 Y5(Note 1), X1 | 17 Y5 (Note 1), X2 | 18 Y5 (Note 1), X3 | 19 Y5 (Note 1), X4 |
|---|---|---|---|---|---|---|---|---|---|
| D | | | | | | | | | |
| A | A | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| T | B | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| A | C | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| O | D | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| U | E (Note 1) | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| T | | | | | | | | | |

**Note 1:** Omit for MM74C922

## Block Diagram



## Absolute Maximum Ratings(Note 2)

| | |
|---|---|
| Voltage at Any Pin | $V_{CC}$ − 0.3V to $V_{CC}$ + 0.3V |
| Operating Temperature Range | |
| MM74C922, MM74C923 | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Operating $V_{CC}$ Range | 3V to 15V |
| $V_{CC}$ | 18V |
| Lead Temperature | |
| (Soldering, 10 seconds) | 260°C |

**Note 2:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CMOS TO CMOS** | | | | | | |
| $V_{T+}$ | Positive-Going Threshold Voltage | $V_{CC}$ = 5V, $I_{IN} \geq$ 0.7 mA | 3.0 | 3.6 | 4.3 | V |
| | at Osc and KBM Inputs | $V_{CC}$ = 10V, $I_{IN} \geq$ 1.4 mA | 6.0 | 6.8 | 8.6 | V |
| | | $V_{CC}$ = 15V, $I_{IN} \geq$ 2.1 mA | 9.0 | 10 | 12.9 | V |
| $V_{T-}$ | Negative-Going Threshold Voltage | $V_{CC}$ = 5V, $I_{IN} \geq$ 0.7 mA | 0.7 | 1.4 | 2.0 | V |
| | at Osc and KBM Inputs | $V_{CC}$ = 10V, $I_{IN} \geq$ 1.4 mA | 1.4 | 3.2 | 4.0 | V |
| | | $V_{CC}$ = 15V, $I_{IN} \geq$ 2.1 mA | 2.1 | 5 | 6.0 | V |
| $V_{IN(1)}$ | Logical "1" Input Voltage, | $V_{CC}$ = 5V | 3.5 | 4.5 | | V |
| | Except Osc and KBM Inputs | $V_{CC}$ = 10V | 8.0 | 9 | | V |
| | | $V_{CC}$ = 15V | 12.5 | 13.5 | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage, | $V_{CC}$ = 5V | | 0.5 | 1.5 | V |
| | Except Osc and KBM Inputs | $V_{CC}$ = 10V | | 1 | 2 | V |
| | | $V_{CC}$ = 15V | | 1.5 | 2.5 | V |
| $I_{rp}$ | Row Pull-Up Current at Y1, Y2, | $V_{CC}$ = 5V, $V_{IN}$ = 0.1 $V_{CC}$ | | −2 | −5 | µA |
| | Y3, Y4 and Y5 Inputs | $V_{CC}$ = 10V | | −10 | −20 | µA |
| | | $V_{CC}$ = 15V | | −22 | −45 | µA |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC}$ = 5V, $I_O$ = −10 µA | 4.5 | | | V |
| | | $V_{CC}$ = 10V, $I_O$ = −10 µA | 9 | | | V |
| | | $V_{CC}$ = 15V, $I_O$ = −10 µA | 13.5 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC}$ = 5V, $I_O$ = 10 µA | | | 0.5 | V |
| | | $V_{CC}$ = 10V, $I_O$ = 10 µA | | | 1 | V |
| | | $V_{CC}$ = 15V, $I_O$ = 10 µA | | | 1.5 | V |
| $R_{on}$ | Column "ON" Resistance at | $V_{CC}$ = 5V, $V_O$ = 0.5V | | 500 | 1400 | Ω |
| | X1, X2, X3 and X4 Outputs | $V_{CC}$ = 10V, $V_O$ = 1V | | 300 | 700 | Ω |
| | | $V_{CC}$ = 15V, $V_O$ = 1.5V | | 200 | 500 | Ω |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 5V | | 0.55 | 1.1 | mA |
| | Osc at 0V, (one Y low) | $V_{CC}$ = 10V | | 1.1 | 1.9 | mA |
| | | $V_{CC}$ = 15V | | 1.7 | 2.6 | mA |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC}$ = 15V, $V_{IN}$ = 15V | | 0.005 | 1.0 | µA |
| | at $\overline{\text{Output Enable}}$ | | | | | |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC}$ = 15V, $V_{IN}$ = 0V | −1.0 | −0.005 | | µA |
| | at $\overline{\text{Output Enable}}$ | | | | | |
| **CMOS/LPTTL INTERFACE** | | | | | | |
| $V_{IN(1)}$ | Except Osc and KBM Inputs | $V_{CC}$ = 4.75V | $V_{CC}$ − 1.5 | | | V |
| $V_{IN(0)}$ | Except Osc and KBM Inputs | $V_{CC}$ = 4.75V | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $I_O$ = −360 µA | | | | |
| | | $V_{CC}$ = 4.75V | 2.4 | | | V |
| | | $I_O$ = −360 µA | | | | |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $I_O = -360\ \mu A$<br>$V_{CC} = 4.75V$<br>$I_O = -360\ \mu A$ | | | 0.4 | V |
| **OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)** | | | | | | |
| $I_{SOURCE}$ | Output Source Current<br>(P-Channel) | $V_{CC} = 5V$, $V_{OUT} = 0V$,<br>$T_A = 25°C$ | −1.75 | −3.3 | | mA |
| $I_{SOURCE}$ | Output Source Current<br>(P-Channel) | $V_{CC} = 10V$, $V_{OUT} = 0V$,<br>$T_A = 25°C$ | −8 | −15 | | mA |
| $I_{SINK}$ | Output Sink Current<br>(N-Channel) | $V_{CC} = 5V$, $V_{OUT} = V_{CC}$,<br>$T_A = 25°C$ | 1.75 | 3.6 | | mA |
| $I_{SINK}$ | Output Sink Current<br>(N-Channel) | $V_{CC} = 10V$, $V_{OUT} = V_{CC}$,<br>$T_A = 25°C$ | 8 | 16 | | mA |

## AC Electrical Characteristics (Note 3)

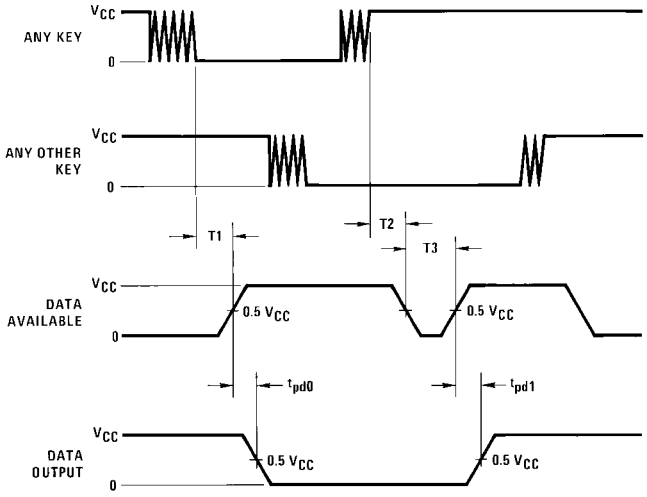
$T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time to | $C_L = 50$ pF (Figure 1) | | | | |
| | Logical "0" or Logical "1" | $V_{CC} = 5V$ | | 60 | 150 | ns |
| | from D.A. | $V_{CC} = 10V$ | | 35 | 80 | ns |
| | | $V_{CC} = 15V$ | | 25 | 60 | ns |
| $t_{0H}$, $t_{1H}$ | Propagation Delay Time from | $R_L = 10k$, $C_L = 10$ pF (Figure 2) | | | | |
| | Logical "0" or Logical "1" | $V_{CC} = 5V$, $R_L = 10k$ | | 80 | 200 | ns |
| | into High Impedance State | $V_{CC} = 10V$, $C_L = 10$ pF | | 65 | 150 | ns |
| | | $V_{CC} = 15V$ | | 50 | 110 | ns |
| $t_{H0}$, $t_{H1}$ | Propagation Delay Time from | $R_L = 10k$, $C_L = 50$ pF (Figure 2) | | | | |
| | High Impedance State to a | $V_{CC} = 5V$, $R_L = 10k$ | | 100 | 250 | ns |
| | Logical "0" or Logical "1" | $V_{CC} = 10V$, $C_L = 50$ pF | | 55 | 125 | ns |
| | | $V_{CC} = 15V$ | | 40 | 90 | ns |
| $C_{IN}$ | Input Capacitance | Any Input (Note 4) | | 5 | 7.5 | pF |
| $C_{OUT}$ | 3-STATE Output Capacitance | Any Output (Note 4) | | 10 | | pF |

**Note 3:** AC Parameters are guaranteed by DC correlated testing.

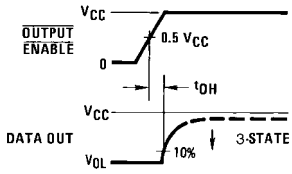
**Note 4:** Capacitance is guaranteed by periodic testing.

## Switching Time Waveforms




T1 ≈ T2 ≈ RC, T3 ≈ 0.7 RC, where R ≈ 10k and C is external capacitor at KBM input.

**FIGURE 1.**



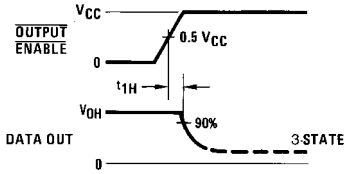
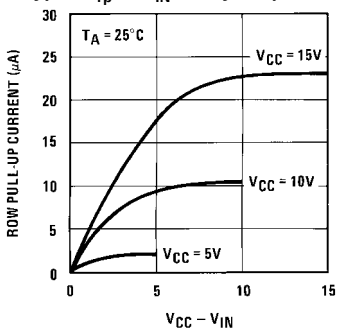



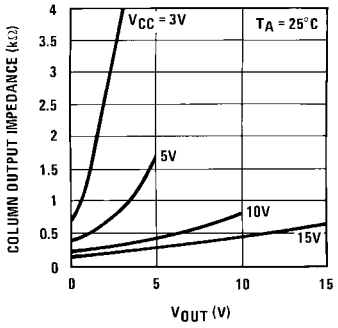

**FIGURE 2.**

## Typical Performance Characteristics

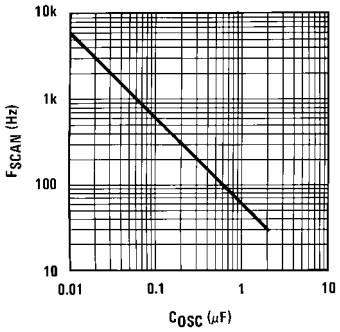
**Typical $I_{rp}$ vs $V_{IN}$ at Any Y Input**



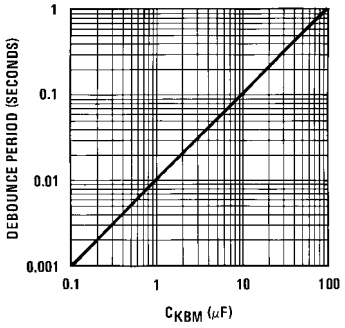

**Typical $R_{on}$ vs $V_{OUT}$ at Any X Output**




**Typical $F_{SCAN}$ vs $C_{OSC}$**

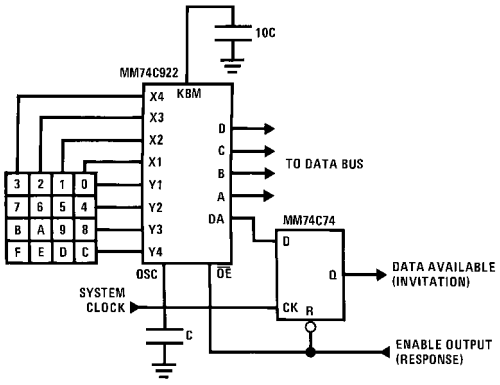



**Typical Debounce Period vs $C_{KBM}$**



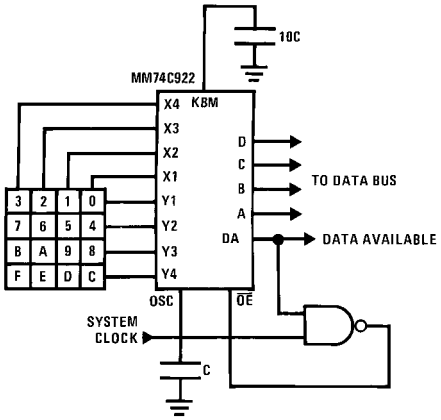

## Typical Applications

**Synchronous Handshake (MM74C922)**




The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

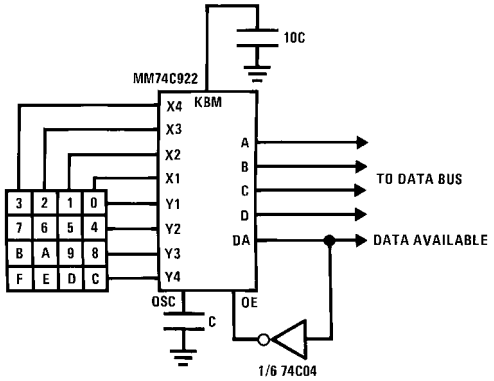
**Synchronous Data Entry Onto Bus (MM74C922)**




Outputs are enabled when valid entry is made and go into 3-STATE when key is released.

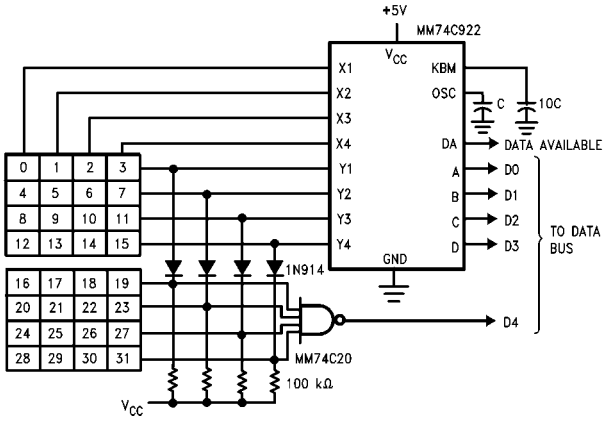
The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

**Asynchronous Data Entry Onto Bus (MM74C922)**




Outputs are in 3-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to 3-STATE.

**Expansion to 32 Key Encoder (MM74C922)**




## Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, $C_{OSE}$, and the key bounce mask capacitor, $C_{MSK}$. Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2–4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

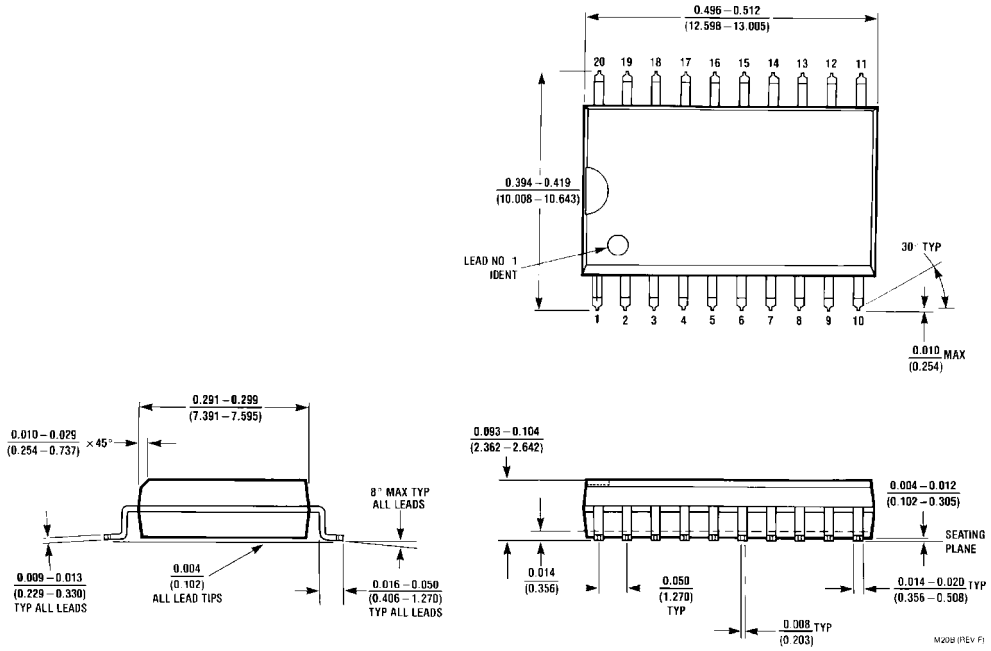
If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

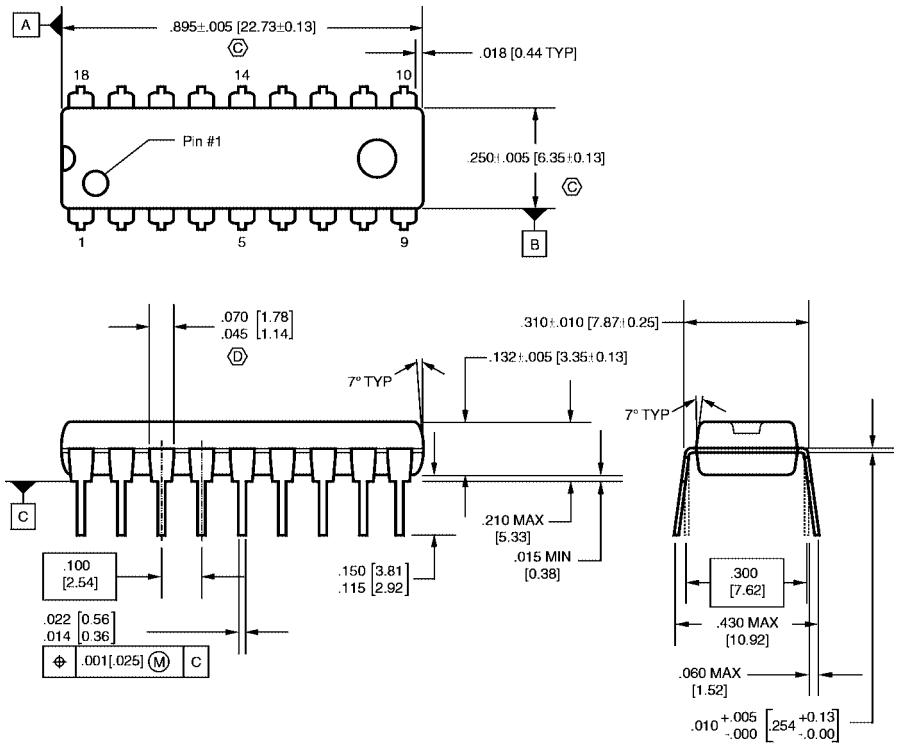
The output latches feed 3-STATE, which is enabled when the Output Enable ($\overline{OE}$) input is taken low.

## Physical Dimensions inches (millimeters) unless otherwise noted




**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**
**Package Number M20B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AC, DATED 6/1993.

B. CONTROLLING DIMENSIONS ARE IN INCHES REFERENCE DIMENSIONS ARE IN MILLIMETERS.

C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.

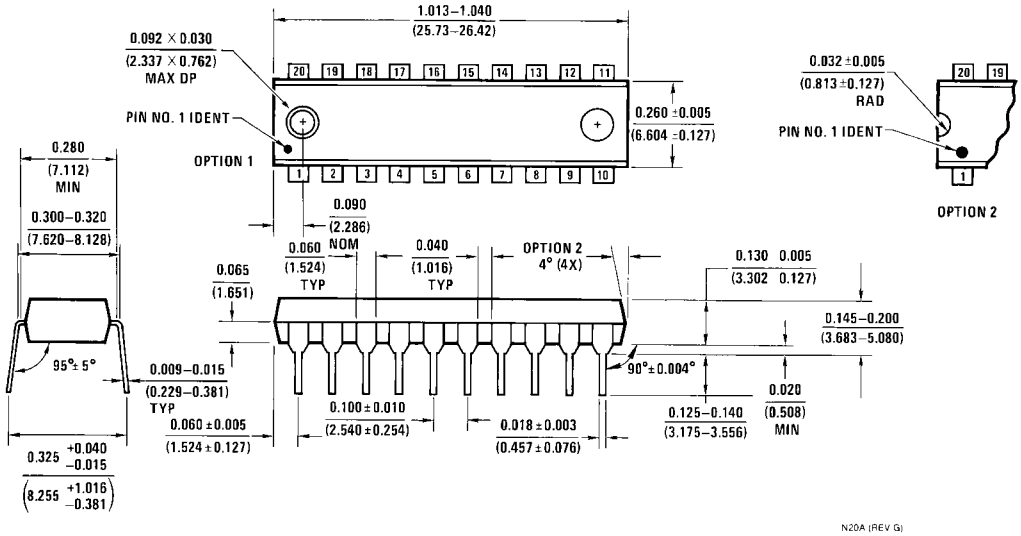
D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.

E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

N18BrevA

**18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N18B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N20A**

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